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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SONG, MATTHEW J	
ART UNIT	PAPER NUMBER
1765	5

DATE MAILED: 01/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/988,233	GRIS ET AL.
	Examiner	Art Unit
	Matthew J Song	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/237,378* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-16, 18, 22, 28-30 and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka (US 4,401,506) in view of Meyerson (US 5,298,452).

Otsuka discloses implanting oxygen ions into a surface of silicon monocrystalline substrate, forming a silicon monocrystalline epitaxial growth layer on the ion implanted surface and conducing a heat treatment (col 2, ln 60 to col 3, ln 55 and claim 3). Otsuka also teaches faults are produced by the ion implantation (col 3, ln 24-26), this reads on defects.

Otsuka is silent to depositing the silicon layer at a temperature less than 750°C.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr and more specifically a deposition temperature of 550°C, this reads on applicant's less than 750°C. Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure and forming a (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Otsuka's method of forming epitaxial silicon with Meyerson process of forming epitaxial silicon at reduced temperatures to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures.

Referring to claim 12 and 33, Otsuka teaches a heat treatment after epitaxial growth, this reads on annealing.

Referring to claims 13-15, Meyerson teaches depositing silicon using silane in a hydrogen carrier gas at a pressure of 10^{-2} to 10^{-4} Torr.

Referring to claims 16, 18, 22 and 38, Otsuka teaches implanting oxygen ions.

Referring to claims 28-30, Otsuka teaches forming a silicon single crystalline layer on a silicon monocrystalline substrate.

Referring to claims 32, the combination of Otsuka and Meyerson is silent to the silicon layer is deposited with a different orientation than that of the substrate. However, since the combination of Otsuka and Meyerson teaches the method claimed, under the principle of inherency the invention, the deposited silicon taught by the combination of Otsuka and Meyerson would inherently have a different orientation than the substrate.

Claim Rejections - 35 USC § 103

3. Claims 11-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,028,556) in view of Meyerson (US 5,298,452).

Chang discloses a substrate **11** comprising silicon is masked and implanted with P+ ions, such as positively charged boron ions, to form a buried layer **13** and silicon is epitaxially grown on top of the substrate and the buried layer and heating the substrate to a predetermined temperature to form wells therein (col 2, ln 35-68 and claim 1). Chang discloses implanting ions into a substrate, as applicant, this inherently causes defects.

Chang is silent to depositing a silicon layer on the region at a temperature of less than 750°C.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr (1.3 to 0.013 Pa). Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure and forming a (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Chang with Meyerson process of forming epitaxial silicon at reduced temperatures to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures.

Referring to claim 12, Chang teach heat treating after epitaxially growing a material on the buried region (claim 1).

Referring to claims 13-15 and 34-37, Meyerson teaches silane and hydrogen at a pressure of 1.3 Pa.

Referring to claims 16, 17, 18, 19, 22, 32, Chang teaches implanting boron ions.

Referring to claims 20, the combination of Chang and Meyerson does not teach implanting with fluorine atoms. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination Chang and Meyerson by using a fluorine dopant because a fluorine dopant is well known in the art.

Referring to claim 21, 24 39, and 41, Chang teaches providing a mask and implanting ions through the mask. Chang is silent to the masking material with a thickness less than 10 nm, but oxide is well known in the art to be used as a masking material. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Chang by using an

oxide mask because oxide is formed at low temperatures and easily patterned. Also, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Chang by conducting routine experimentation to determine the optimal mask thickness. Chang is silent to the mask is removed, but in Fig 4, the masking material is not present. Therefore Chang inherently incorporates a step to remove the masking.

Referring to claim 29, Chang is silent to the crystallinity of the substrate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Chang by using a single crystalline substrate because single crystalline substrates have improved conductivity characteristics over amorphous substrates.

Referring to claims 27 and 32, the combination of Chang and Meyerson is silent to the silicon layer is deposited with a different orientation than that of the substrate. However, since the combination of Chang and Meyerson teaches the method claimed, under the principle of inherency the invention is considered to be anticipated by the combination of Chang and Meyerson.

Referring to claims 23 and 40, the combination of Chang and Meyerson does not teach the density of interstitial defects. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang and Meyerson by conducting routine experimentation to determine the optimum amount of interstitial defects per one hundred silicon atoms.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 11, 16, 17, 19, 20, 21, 23-32, 34, 35 and 38-42 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,165,265. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 11, 16, 17, 19, 20, 23, 25-30, 32, 34 and 35 are generic to the method recited in claims 1-8 of US 6,165,265. That is, claims 1-8 of US 6,165,265 falls entirely within the scope of claims 11, 16, 17, 19, 20, 23, 25-30, 32, 34 and 35, or, in other words, claims 11, 16, 17, 19, 20, 23, 25-30, 32, 34 and 35 are anticipated by claims 1-8 of US 6,165,265. Specifically, since interstitial defects are a species of he generics category defined by "defects", the process of claims 11, 16, 17, 19, 20, 23, 25-30, 32, 34 and 35 reciting "defects" is anticipated by claims 1-8 of US 6,165,265 reciting "interstitial defects".

6. Claims 13-15 and 36-37 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,165,265 in view of Meyerson (US 5,298,452).

Claims 1-8 of US 6,165,265 recites a recites a method of depositing a silicon layer on a single crystal silicon substrate, so that the silicon layer is a single crystal layer, but of different orientation than the substrate, including the steps of creating interstitial defects with an atomic proportion lower than one for one hundred and performing a silicon deposition in condition generally corresponding to those of an epitaxial deposition, but at a temperature lower than 750°C. Claims 1-8 of US 6,165,265 also recites an implantation step for forming defects, a silicon oxide layer of thickness lower than 10 nm, implanting with an electrically neutral element of fluorine and the window opening has a width lower than 5 micrometers

However, US 6,165,265 is silent to the atmosphere of the silicon deposition.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr. Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the method of claims 1-8 of US 6,165,265 with Meyerson to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures.

7. Claims 12, 18, 22 and 33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,165,265 in view of Otsuka (US 4,401,506). US 6,165,265 recites all of the limitations of claim 12, as discussed previously, except depositing a silicon layer at a temperature prior to annealing the wafer.

Otsuka teaches implanting oxygen ions into a surface of silicon monocrystalline substrate, forming a silicon monocrystalline epitaxial growth layer on the ion implanted surface and conducing a heat treatment (col 2, ln 60 to col 3, ln 55 and claim 3). Otsuka also the steps of ion implantation and heat treatment may be conducted in the reverse order (col 3, ln 30-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify US 6,165,265 with Otsuka's annealing after depositing a Silicon layer to produce microdefects in the ion implanted surface, which absorb impurities in the surface of the substrate (col 1, ln 35-60 and claim 3).

Referring to claims 18 and 22, Otsuka teaches implanting oxygen ions.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Plumton (US 5,554,561) teaches that doping by implantation affects the crystal orientation of GaAs grown on GaAs (col 1, ln 60-67 and col 7, 50-67).

Wu et al (US 4,584,0296) teaches implanting fluorine into a silicon substrate to make the surface of the substrate amorphous (col 3, ln 1-30) because fluorine decreases the temperature at which an effective level of conductivity is achieved (Example 1).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 703-305-4953. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin L Utech can be reached on 703-308-3868. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song
Examiner
Art Unit 1765

MJS
January 17, 2003

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